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EXAMINER	
RYMAN, DANIEL J	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/621,315	SIKKINK ET AL.
	Examiner	Art Unit
	Daniel J. Ryman	2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12 November 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,3-6,8-10,14-16 and 18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3-6,8-10,14-16 and 18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 November 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/12/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/12/2005 have been fully considered but they are not persuasive. On pages 10-12, Applicant alleges that the references do not contain certain features, such as the use of a secondary synch pulse. However, Applicant does not explain why Khandekar's mask signal, which Examiner equates with Applicant's secondary synch pulse, is patentably distinct from Applicant's secondary synch pulse. Absent such an explanation, Examiner is not convinced that the pending claims are patentably distinct.

2. Further, on pages 11-12, Applicant contends that "there is no teaching or suggestion in Khandekar or in any of the other cited references to apply the approach described by Khandekar to the circuit described by Huon." Examiner, respectfully, disagrees. Examiner has explicitly provided the following motivation for the combination: "in order to check for skew between the two clock signals (Fig. 5 and col. 7, line 38-col. 8, line 28, esp. col. 7, line 66-col. 8, line 10)." In addition, Khandekar discloses in further passages cited by Examiner that "[a] synchronous transfer mechanism may accordingly introduce a reduced transfer latency penalty . . . than an asynchronous transfer mechanism." Col. 1, lines 50-56. Thus, Khandekar suggests the combination in order to provide a synchronous transfer mechanism, which will introduce a reduced latency penalty, and which compensates for clock skew. As such, Examiner maintains that the rejection is proper.

Claim Objections

3. Claim 1 is objected to because of the following informalities: in line 2, "at by a" should be "by a". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-6, 8-10, 14-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huon et al (USPN 5,761,735) in view of Duffy (USPN 6,535,527) in further view of Santahuhta (EP 0989484) in further view of Khandekar et al (USPN 6,049,887).

6. Regarding claim 1, Huon discloses an interface for data transfer from a first domain clocked by a first clock at a first frequency to a second domain clocked by a second clock at a slower frequency, comprising: a first register for receiving data from the first domain when the first register is selected (col. 1, line 66-col. 2, line 19 and col. 3, line 50-col. 4, line 4); a second register for receiving data from the first domain when the second register is selected (col. 1, line 66-col. 2, line 19 and col. 3, line 50-col. 4, line 4); and a third register for transferring data from said first register or said second register to the second domain when the second domain is clocked by a clock pulse of the second clock (col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7), said third register being selectively toggled to receive data from said first register or said second register upon a clock pulse (col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7).

Huon does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line 9). In addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on the falling

edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Huon read and write data according to a clock signal where latches read and write data according to a clock signal.

Further, Huon in view of Duffy does not expressly disclose that the third latch is selectively toggled in response to a negative edge of the clock pulse clocking the second domain; however, Huon in view of Duffy does disclose that the third latch is selectively toggled in response to a clock pulse from a processor clock (Huon: col. 4, lines 31-32 and col. 7, lines 19-22). Santahuhta teaches, in a system for synchronizing a data stream, selectively toggling the read of two latches in response to a negative edge of the clock pulse clocking the second domain (col. 4, lines 33-48 and col. 5, lines 21-39) where the toggling is controlled by a processor with a clock input (Fig. 3, ref 304; Fig. 4, ref. 106 and 107; col. 2, line 54-col. 3, line 13; and col. 4, lines 33-48) since a latch has data read from it on the falling edge of a clock signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the third latch be alternately toggled in response to a negative edge of the clock pulse clocking the second domain, other than a hold pulse, since latches have data read from them on the falling edge of a clock signal.

Huon in view of Duffy in further view of Santahuhta does not expressly disclose that the first clock clocking the first domain and the second clock clocking the second domain are both

derived from a single primary clock and generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock. Khandekar teaches, in a system for transferring a signal between two synchronous clock domains, having a first clock clocking the first domain and a second clock clocking the second domain be both derived from a single primary clock (Figs. 3 and 5, common oscillator) in order to ensure that both clock domains are synchronized which simplifies circuitry needed to transfer signals between the domains (col. 1, lines 35-67) and generating clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock (mask signal) in order to check for skew between the two clock signals (Fig. 5 and col. 7, line 38-col. 8, line 28, esp. col. 7, line 66-col. 8, line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to transfer a signal between two synchronous clock domains, having a first clock clocking the first domain and a second clock clocking the second domain be both derived from a single primary clock in order to ensure that both clock domains are synchronized which simplifies circuitry needed to transfer signals between the domains and to generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock in order to check for skew between the two clock signals.

7. Regarding claim 3, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that at least one clock pulse of the first domain clock is a non-operate (NOP) clock pulse in each repeated systematic pattern when no data from the first domain is loaded into either said first latch or said second latch to cause equal average data transfer

between the first domain and the second domain (Santahuhta: col. 6, lines 14-46 and Khandekar: abstract; col. 4, lines 12-37; and col. 4, line 47-col. 5, line 8).

8. Regarding claim 4, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that the NOP clock pulse is selected to minimize latency and prevent the slower clocked domain from being overrun by the faster clocked domain (Santahuhta: col. 6, lines 14-46 and Khandekar: abstract; col. 4, lines 12-37; and col. 4, line 47-col. 5, line 8).

9. Regarding claim 5, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar discloses that the first and second latches are alternately selected by a select signal, said select signal being generated to select one of said first or second latches when the other of said first or second latches receives data (Huon: col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7).

10. Regarding claim 6, Huon discloses an interface for data transfer between a first domain clocked at one frequency and a second domain clocked at a faster frequency, comprising: a first register for receiving data from the first domain when the first register is selected (col. 1, line 66-col. 2, line 19 and col. 3, line 50-col. 4, line 4); a second register for receiving data from the first domain when the second register is selected (col. 1, line 66-col. 2, line 19 and col. 3, line 50-col. 4, line 4); and a third register selectively toggled to receive data from said first register or said second register upon a clock pulse, other than a hold pulse (col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7), said third register transferring data from said first latch or said second register to the second domain when the second domain is clocked by a next clock pulse that is not a hold clock pulse (col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7).

Huon does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line 9). In addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on the falling edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Huon read and write data according to a clock signal where latches read and write data according to a clock signal.

Further, Huon in view of Duffy does not expressly disclose that the third latch is selectively toggled in response to a negative edge of the clock pulse clocking the second domain; however, Huon in view of Duffy does disclose that the third latch is selectively toggled in response to a clock pulse from a processor clock (Huon: col. 4, lines 31-32 and col. 7, lines 19-22). Santahuhta teaches, in a system for synchronizing a data stream, selectively toggling the read of two latches in response to a negative edge of the clock pulse clocking the second domain (col. 4, lines 33-48 and col. 5, lines 21-39) where the toggling is controlled by a processor with a clock input (Fig. 3, ref 304; Fig. 4, ref. 106 and 107; col. 2, line 54-col. 3, line 13; and col. 4, lines 33-48) since a latch has data read from it on the falling edge of a clock signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the third latch be alternately toggled in response to a negative edge of the clock

pulse clocking the second domain, other than a hold pulse, since latches have data read from them on the falling edge of a clock signal.

Huon in view of Duffy in further view of Santahuhta does not expressly disclose that the first clock clocking the first domain and the second clock clocking the second domain are both derived from a single primary clock and generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock. Khandekar teaches, in a system for transferring a signal between two synchronous clock domains, having a first clock clocking the first domain and a second clock clocking the second domain be both derived from a single primary clock (Figs. 3 and 5, common oscillator) in order to ensure that both clock domains are synchronized which simplifies circuitry needed to transfer signals between the domains (col. 1, lines 35-67) and generating clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock (mask signal) in order to check for skew between the two clock signals (Fig. 5 and col. 7, line 38-col. 8, line 28, esp. col. 7, line 66-col. 8, line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to transfer a signal between two synchronous clock domains, having a first clock clocking the first domain and a second clock clocking the second domain be both derived from a single primary clock in order to ensure that both clock domains are synchronized which simplifies circuitry needed to transfer signals between the domains and to generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock in order to check for skew between the two clock signals.

11. Regarding claim 8, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that the hold clock pulse is selected to minimize latency since the hold clock pulse (reset) delays the second domain data read until data is available to read (Santahuhta: col. 6, lines 14-46).

12. Regarding claim 9, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar discloses that the first and second latches are alternately selected by a select signal, said select signal being generated to select one of said first or second latches when the other of said first or second latches receives data (Huon: col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7).

13. Regarding claim 10, Huon discloses an interface for data transfer between domains clocked at different frequencies, comprising: a first register for receiving data from a first domain clocked at one frequency when said first register is selected (col. 1, line 66-col. 2, line 19 and col. 3, line 50-col. 4, line 4); a second register for receiving data from the first domain when said second register is selected (col. 1, line 66-col. 2, line 19 and col. 3, line 50-col. 4, line 4); and a third register for transferring data from either said first register or said second register to a second domain clocked at another frequency (col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7), wherein the first domain is clocked at a slower frequency than the second domain (col. 4, lines 10-20 and col. 7, line 66-col. 8, line 7).

Huon does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line 9). In addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on the falling

edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Huon read and write data according to a clock signal where latches read and write data according to a clock signal.

Huon in view of Duffy in further view of Santahuhta does not expressly disclose that the third register is loaded when the second domain is clocked by a clock pulse that is not a non-operate pulse since Huon in view of Duffy in further view of Santahuhta does not expressly disclose the use of a non-operate pulse. Khandekar teaches that at least one clock pulse of the first domain clock is a non-operate (NOP) clock pulse in each repeated systematic pattern when no data from the first domain is loaded into either said first latch or said second latch to correct for clock skew (Khandekar: abstract; col. 4, lines 12-37; and col. 4, line 47-col. 5, line 8). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to load the third register when the second domain is clocked by a clock pulse that is not a non-operate pulse in order to eliminate clock skew.

14. Regarding claim 14, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar discloses that the third latch is alternately toggled to transfer data from said first or said second latch in response to a negative edge of a clock pulse clocking the second domain unless the clock pulse is a non-operate clock pulse (Santahuhta: Fig. 3, ref 304; Fig. 4, ref. 106

and 107; col. 2, line 54-col. 3, line 13; col..3, line 25-col. 4, line 11; col. 4, lines 33-48; col. 5, lines 21-39; and col. 6, lines 14-46).

15. Regarding claim 15, Huon discloses a method for data transfer between clocked domains, comprising: loading a first master register with data from the first domain in response to a first domain clock pulse (col. 1, line 66-col. 2, line 19 and col. 3, line 50-col. 4, line 4); transferring the data loaded in the first master register to the second domain through a slave register in response to a second domain clock pulse (col. 1, line 66-col. 2, line 19; col. 3, line 50-col. 4, line 4; col. 4, lines 10-20; and col. 7, line 66-col. 8, line 7); toggling the slave register to switch to receive data from a second master register (col. 1, line 66-col. 2, line 19; col. 3, line 50-col. 4, line 4; col. 4, lines 10-20; and col. 7, line 66-col. 8, line 7); loading the second master register with data from the first domain in response to another first domain clock pulse (col. 1, line 66-col. 2, line 19; col. 3, line 50-col. 4, line 4; col. 4, lines 10-20; and col. 7, line 66-col. 8, line 7); transferring the data loaded in the second master register to the second domain through the slave register in response to another second domain clock pulse (col. 1, line 66-col. 2, line 19; col. 3, line 50-col. 4, line 4; col. 4, lines 10-20; and col. 7, line 66-col. 8, line 7); toggling the slave register to switch to receive data from the first master register (col. 1, line 66-col. 2, line 19; col. 3, line 50-col. 4, line 4; col. 4, lines 10-20; and col. 7, line 66-col. 8, line 7); repeating a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register (col. 1, line 66-col. 2, line 19; col. 3, line 50-col. 4, line 4; col. 4, lines 10-20; and col. 7, line 66-col. 8, line 7).

Huon does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line 9). In

addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on the falling edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Huon read and write data according to a clock signal where latches read and write data according to a clock signal.

Further, Huon in view of Duffy does not expressly disclose that the slave latch is alternately toggled in response to a negative edge of the clock pulse clocking the second domain; however, Huon in view of Duffy does disclose that the slave latch is alternately toggled in response to a clock pulse from a processor clock (col. 4, lines 31-32 and col. 7, lines 19-22). Santahuhta teaches, in a system for synchronizing a data stream, alternately toggling the read of two latches in response to a negative edge of the clock pulse clocking the second domain (col. 4, lines 33-48 and col. 5, lines 21-39) where the toggling is controlled by a processor with a clock input (Fig. 3, ref 304; Fig. 4, ref. 106 and 107; col. 2, line 54-col. 3, line 13; and col. 4, lines 33-48) since a latch has data read from it on the falling edge of a clock signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the slave latch be alternately toggled in response to a negative edge of the clock pulse clocking the second domain; other than a non-operate clock pulse, since latches have data read from them on the falling edge of a clock signal.

Additionally, Huon in view of Duffy does not expressly disclose repeating a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register until a master clear signal is received by the slave and master registers; and entering a non-operate state during each repeated cycle for at least one clock pulse of the faster domain clock, if the domains are clocked at different frequencies. Santahuhta teaches, in a system for synchronizing a data stream, repeating a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register until a master clear signal (reset) is received by the slave and master registers; and entering a non-operate state during each repeated cycle for at least one clock pulse of the faster domain clock, if the domains are clocked at different frequencies since the reset is required if not enough data has entered the system when the first domain is slower than the second domain in order to allow the first domain to catch up to the second domain (col. 6, lines 14-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to repeat a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register until a master clear signal (reset) is received by the slave and master registers; and enter a non-operate state during each repeated cycle for at least one clock pulse of the faster domain clock, if the domains are clocked at different frequencies since a reset is required if not enough data has entered the system when the first domain is slower than the second domain in order to allow the first domain to catch up to the second domain.

Huon in view of Duffy in further view of Santahuhta does not expressly disclose that the clock pulses of the first domain and the second domain are both derived from a primary clock and repeat in a ratioed, systematic pattern framed by a secondary synch pulse. Khandekar

teaches, in a system for transferring a signal between two synchronous clock domains, having a first clock clocking the first domain and a second clock clocking the second domain be both derived from a single primary clock (Figs. 3 and 5, common oscillator) in order to ensure that both clock domains are synchronized which simplifies circuitry needed to transfer signals between the domains (col. 1, lines 35-67) and generating clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock (mask signal) in order to check for skew between the two clock signals (Fig. 5 and col. 7, line 38-col. 8, line 28, esp. col. 7, line 66-col. 8, line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to transfer a signal between two synchronous clock domains, deriving both of the clock pulses of the first domain and the second domain from a primary clock and repeating the pulses in a ratioed, systematic pattern framed by a secondary synch pulse in order to check for skew between the two clock signals.

16. Regarding claim 16, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar discloses generating a signal in response to loading one of the first or second master latches to cause data to be loaded alternately into the first and second master latches (Huon: col. 1, line 66-col. 2, line 19; col. 3, line 50-col. 4, line 4; col. 4, lines 10-20; and col. 7, line 66-col. 8, line 7 and Santahuhta: col. 4, lines 33-48 and col. 5, lines 21-39).

17. Regarding claim 18, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that the non-operate state is selected to minimize latency in transferring the data between the domains since the hold clock pulse (reset) delays the second domain data read until data is available to read (Santahuhta: col. 6, lines 14-46).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Manning (USPN 6,000,022) see col. 6, line 52-col. 7, line 38, esp. col. 7, lines 33-37 which pertains initiating a non-operate pulse to minimize latency. Bryant et al (USPN 6,535,946) see entire document which pertains to synchronizing data transfers between clock domains derived from a common clock. Rios (USPN 5,256,912) see entire document which pertains to synchronizing data transfers between clock domains. Taylor (USPN 5,758,131) see entire document which pertains to synchronizing data transfers between clock domains.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 7:00-4:30 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJR

Daniel J. Ryman
Examiner
Art Unit 2665

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600